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Design of Low Power Pulse Triggered Flip-Flop Using DCPT

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***Abstract*— Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption in VLSI circuits. In any integrated circuit flip–flop consumes large amount of power as they make maximum number of internal transitions. This paper presents a high performance, energy efficient implicit pulsed triggered flip flop based on direct coupled pass transistor (DCPT) approach. This approach directly couple input D to output Q of the flip flop to alleviate the worst case delay. It reduces input to output travelled path hence reduces D-to-Q delay and power consumption. It also includes an extra NMOS for latch designing to reduce the crossbar current. The simulation results presented are obtained by using Tanner EDA tool. By this technique it improves delay and power dissipation for the proposed implicit pulsed flip flop.**

Keywords— Flip-flop, Low Power, Pulse Triggered.

I. INTRODUCTION

The flip flops (FFs) are the basic memory blocks used in all types of digital designs. It is evaluated that the power dissipation by the clock system, which comprise of clock distribution network and storage components, is as high as 20% to 45% of the overall system power. Pulse-triggered flip flops (P-FFs) are considered an alternative to the conventional master-slave flip flops (MS-FFs). In contemporary synchronous digital system both MS-FFs and P-FFs are commonly used. Conventional MS-FFs consists of cascaded master and slave latches, so require a positive setup time that increases the input to output delay. A P-FF consists of a pulse generator for generating narrow transparency window and a latch for data storage. As transparency window generated on either of the rising or falling edge of the clock signal are very narrow, the latch so formed acts like an edge-triggered flip flop. So zero or negative setup time is allowed for P-FFs. The P-FFs are also having less complicated circuit as it uses only one latch than conventional MS-FFs which needs two latches. This leads speed advantage as well as lowering the power consumption of the flip flop system. Based on transparency window generation, P-FFs are classified as the explicit P-FF (EP-FF) and the implicit P-FF (IP-FF). This characterization is based on pulse generation. In implicit type, pulse generation is done inside the flip flop. In explicit type flip flop the pulse is externally generated.

An external pulse generator circuit is used to generate transparency window in EP-FFs, which is used as the central clock for all neighboring flip flops. This has an advantage over power overhead of the pulse generator but the generated pulse could be difficult to manage practically due to the increased capacitive load at the clock node. An IP-FF gives better control of transparency window width as the pulse generator is incorporated into FF structure itself.

Here, we are mainly focusing on designing the IP-FF for ultra-low power dissipation and high performance. The proposed technique uses pass transistor to provide a direct coupling of input D to the output Q by providing minimum delay and reduced power dissipation by reducing number of switching transistors. The proposed approach leads to reduced power consumption for higher input data switching activity and comparable for lower data switching activity.

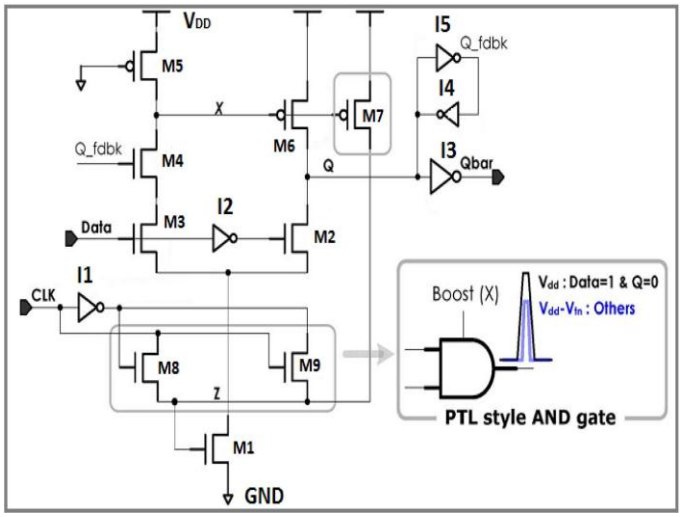

Fig.1. Conditional Pulse Enhancement IP-FF .

II. CONVENTIONAL IMPLICIT PULSED TRIGGERED FLIP-FLOPS

In implicit type flip-flops the clock distribution circuit is a built in logic and there is no need for an external circuitry for the clock division and distribution. Implicit type flip-flops consist of two parts, a clock distribution network or clock tree and a latch for data storage. Several low power techniques are available which can be applied to the pulse flip-flops they are conditional enhancement, conditional capture and conditional data mapping. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch.

A. *Conditional Pulse Enhancement Flip-Flop*

Fig.1 shows the conditional pulse enhancement flip-flop (CPE-FF). It uses M7 to conditionally enhance the discharging strength when input D is 1. It consists of two parts, first the discharging path of node X having clocked transistor M I and second a simple latch consists of inverters 14 and 15. It uses 2-input pass transistor logic (PTL) based AND gate to generate sharp pulse of short duration to control the discharge 0 node X through transistor MI. Most of the time, input to AND logic of the clock network is either 0 or 1 so gives node Z as 0 except for transition edges of the clock. Pulse is generated when both the transistors M8 and M9 are ON at the same time for very short duration and the pulse generated has a pulse width equal to the delay of the inverter 11.

In this design, a simple latch is used to store the state of the node Q for future use. This latch design suffers from crossbar leakage current. Crossbar current occur when node Q_fdbk is transitioning from high to low and Q from low to high, as PMOS transistor takes some time to transition from high to low, there is a time when both transistors of inverter 14 turns ON. This causes extra power loss as crossbar leakage.

This design has transistor MI and M2 for discharging node Q to 0 for transparency window. For pulling down the node Q, it uses inverter 12, transistors MI and M2. The proposed design removes inverter from the discharging path to give a direct path from input D to the output Q (direct signal feed-through). For pulling up the node Q, it makes transistor M6 to turn ON and node Q is directly connected to the supply voltage V_{DD}. For this design, pull-up path contributes to the critical path of the design. It occurs when input D is I and output Q is O. To enhance the critical path, it uses transistor M7. Whenever critical path occurs, node X becomes low and turns ON the transistor M7. Now this transistor connect node Z to V_{DD} and enhance the driving capability of transistor Ml. Most of the time node X is connected to V_{DD} through always ON pull-up transistor MS. So transistor M7 is OFF most of the time. It only turns ON when a boost is needed to MI during critical path case.

B. *Contention Reduced Pulse triggered IP-FF*

Fig. 2 shows the contention reduced conditional pulse enhancement pulse triggered flip flop (CR-CPEFF). This FF uses some circuital modifications to reduce the current contention (CC) during critical path switching of IP-FFs. To reduce CC, this design uses two parallel PMOS network (MII, MI2) instead of always ON PMOS transistor used in CPE-FF. These CC reduction transistors are conditionally controlled by signals Q and Q_fdbk. Here MIS is used to avoid crossbar leakage current. The problem with this design is increased load capacitance at node X due to extra PMOS. It also increases the parasitic capacitances at node Q and Q_fdbk. To reduce the load capacitance at node X, an always ON pull-up transistor is used in proposed design.

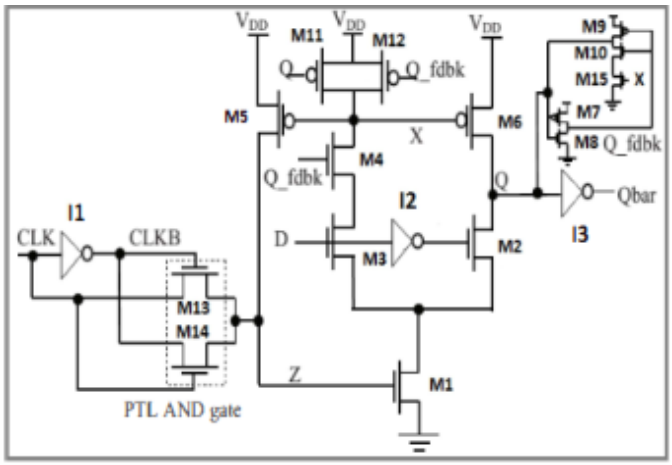

Fig.2. Contention Reduced Pulse triggered IP-FF

III. PROPOSED FLIP-FLOP DESIGN

Reviewing the conventional FFs in previous section, it is observed that all P-FFs are suffering from the worst case delay occurring at critical switching of node Q from 0 to 1. Fig. 3 shows the proposed DCPT based pulse triggered flip flop design. It uses the DCPT scheme to overcome the challenges of conventional IP-FF designs. By using DCPT scheme, it reduces the path from input to output by providing a direct path from input to output to improve the delay constraints. This design employs the concept of PTL based AND logic for pulse generation. For transparency window, critical path is formed while charging of node Q through M7 when high input is applied. To overcome the critical path delay during low to high transition of Q, two approaches are used. First is, it employs transistor M6 to provide an extra boost to increase the driving capability of

both transistors MI and M2 & the second is the boost provided by transistor M2 used as DCPT.

Proposed design uses an extra transistor MI2 controlled by node voltage X to remove the crossbar current problem of CPE-FF. It uses conditional discharge technique to avoid redundant switching of internal nodes. When input is high and output Q is also high, then there is no need of switching Q to high as it is already in high state. This is ensured by M4 controlled by Q_fdbk signal. This saves switching power by reducing the number of switching transistors. Compared to CPE-FF and CR-CPEFF, the proposed IP-FF reduces the number of transistor leading to lesser area overhead. For discharging the node Q, it uses only transistor M2. When clock pulse arrives, transistor M2 turns ON by connecting input D to the output Q directly. Here transistor M2 acts as a connector between input and output which is controlled by pulse generated at the rising edge of the clock. Transistor M2 works well for both inputs 0 and 1. For input 0, it directly couples input to the output with minimum possible delay and for input I, it provide extra driving strength to output node Q.

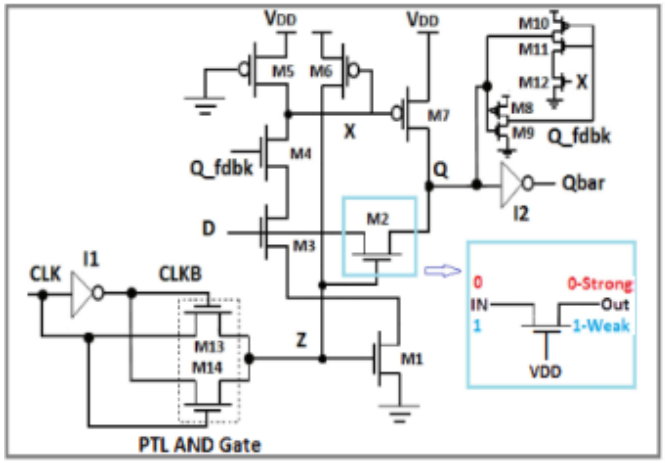

Fig.3. Proposed Direct Coupled Pass Transistor based IP-FF.

The clock pulse is generated for rising transition of the input clock signal. This clock pulse is used as the transparency window for the operation of the FF. The working principle of the proposed design is explained as follows. Let beginning of the operation, D and Q are at logic transparency window, when applied input D is 0 and transistor M2 is turned ON there is a direct path from input to output resulting Q to be 0 with minimum possible delay. If Q is 1 and applied input is 0 for transparency window, then also M2 provide direct path for D to Q making Q to logic o. When applied input is I and Q is 0 for transparency window then QJdbk is 1 and the worst case path is formed by turning ON transistor M4, M3 and MI. This will discharge node X to 0 by pull-up transistor M7, which connect node Q to V_{DD}. To improve the worst case delay two schemes are used here. First one is the use of transistor M6 to provide a boost by increasing the strength of the pulse when D is I and Q is O. The second is the use of M2 for directly coupling input to the output Q for providing an extra boost in worst case.

IV. EXPERIMENTAL RESULTS

The Proposed Direct Coupled Pass Transistor based IP-FF is designed by using Tanner EDA tool and the results are analyzed. The simulations are done for proper applied capacitive load. Fig.5. shows the simulation waveform for the proposed DCPT based IP-FF. The waveform shows that for rising clock signal, a pulse of magnitude V_{DD}-Vth is generated that triggers the switching of the output signal Q according to the input signal D. Power waveform shows power dissipated whenever there is a switching of signals.

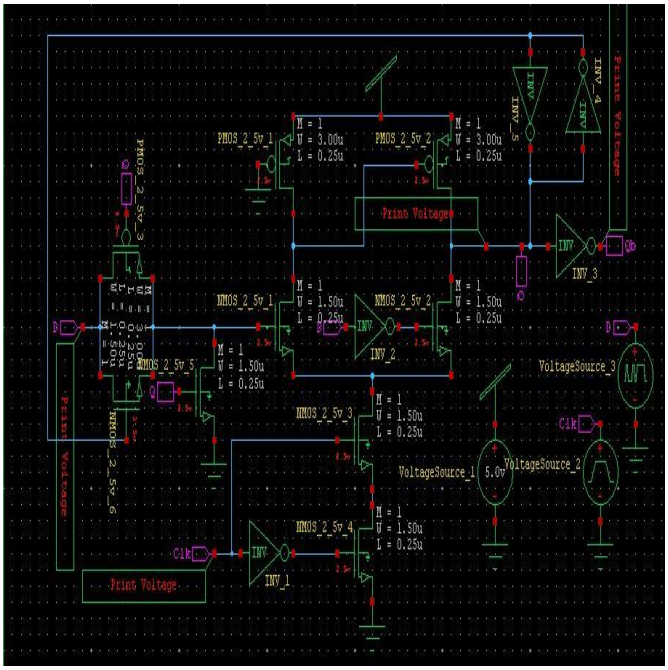

Fig.4. Schematic view of Proposed Direct Coupled Pass Transistor based IP-FF.

TABLE.1

COMPARISON RESULT

	CPE-FF	CR-CPEFF	PROPOSED IP-FF
Technology	250nm	250nm	250nm
Power (mW)	5.28	4.98	4.52
No. of Transistors	19	21	18

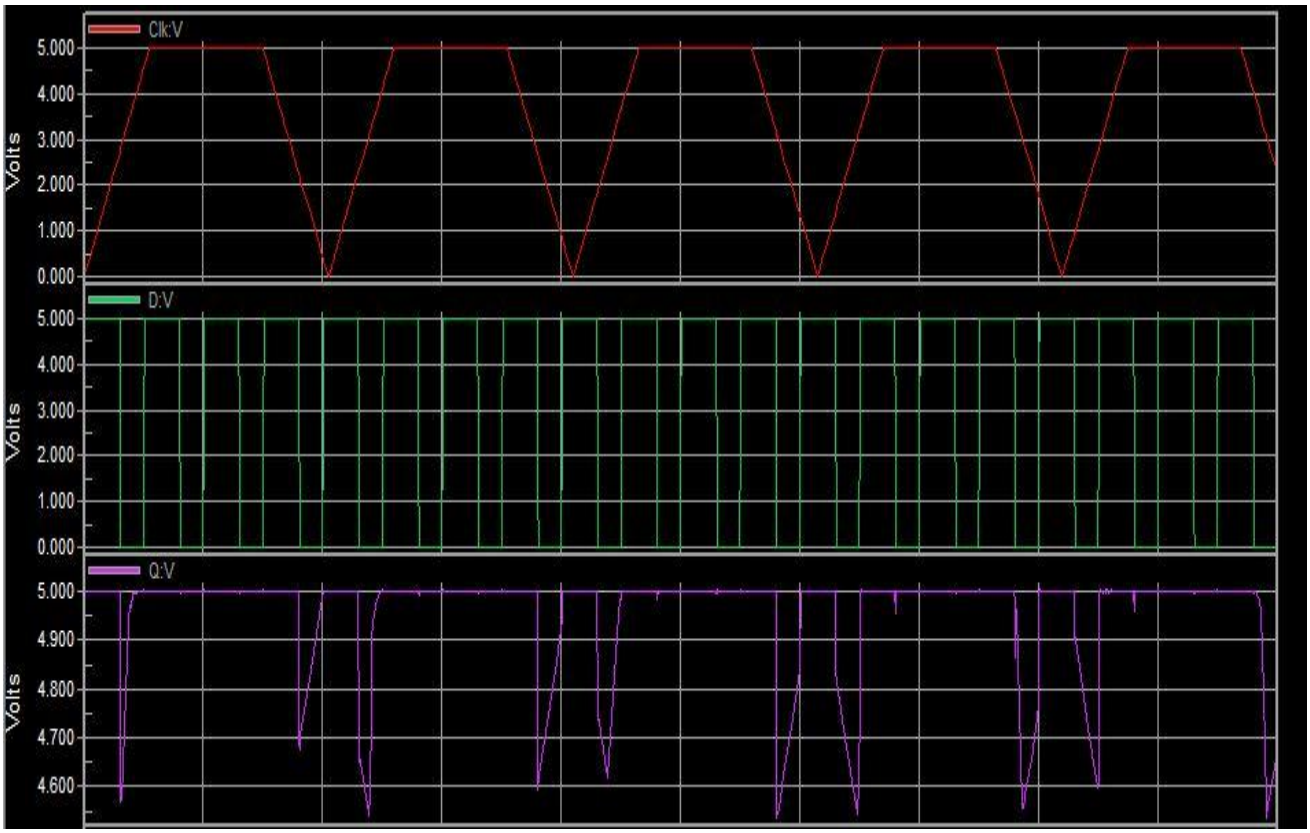

Fig.5. Simulation Waveform of Proposed Direct Coupled Pass Transistor based IP-FF.

The table 1 shows the comparison results of proposed implicit pulse triggered flip-flop (IP-FF) with the previous type Conditional Pulse Enhancement Flip-Flop (CPFF) and Contention Reduced Pulse triggered IP-FF (CR-CPEFF). While comparing these we concluded that the proposed design is efficient in both power and area.

V. CONCLUSION

It is reviewed that most of the IP-FFs suffer from worst case delay due to critical path. This worst case delay affects 0- to-Q delay and PDP. In this paper a simple direct couple pass transistor (DCPT) based IP-FF is presented to alleviate the worst case D-to-Q delay and PDP. It also reduces power by improving crossbar leakage current in the latch design. The simulation results support the claim of the proposed design using various performance aspects. Proposed design improves delay by 2% and PDP by 22%. It also uses less number of transistors than other conventional designs.

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