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An Efficient Design of Low Power Shift Register using Pulsed Latches

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***Abstract*— Now-a-days for each and every designing in VLSI era the power consumption plays a vital role. Low power has emerged as a principal theme in today's electronics industry. The low power VLSI design has important role in designing of many electronic design systems. On designing any combinational or sequential circuits, the power consumption, implementation area, voltage leakage, and efficiency of the circuit are the important parameters to be considered initially.**

This paper proposes a low power and efficient area shift register by using pulsed latches. The power and area is reduced by replacing flip flop with pulsed latches. This is also solves the timing problem non overlap delayed signal instead of conventional signal. The shift register uses a less number of pulsed clock signals by grouping latches to several sub system and using additional temporary latches. A shift register using pulsed latches is reduced the area and power. The proposed shift register saves the power and area compared to conventional shift register with flip flop. Also the shift register uses a small number of the pulsed clock signals by grouping the latches to more than a few sub shifter registers and using supplementary temporary storage latches.

Keywords— Flip-flop, Pulsed clock, Pulsed latch, Shift register.

I. INTRODUCTION

A Shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs.

An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-mega- pixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increase the area and power consumption of the shift register become important design considerations.

The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption, because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

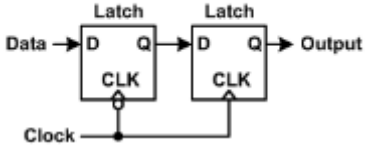

Fig.1(a) Master Slave Flip-Flop.

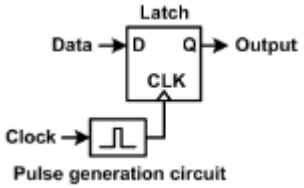

Fig.1(b) Pulse Generation Circuit.

II. ARCHITECTURE

A. Proposed Shift Register

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

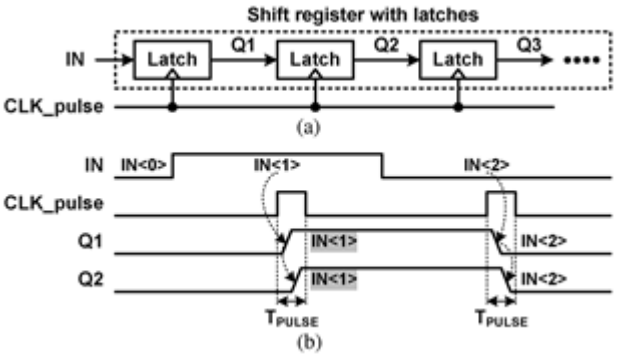

Fig.2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width, but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. How-ever, the delay circuits cause large area and power overheads.

Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

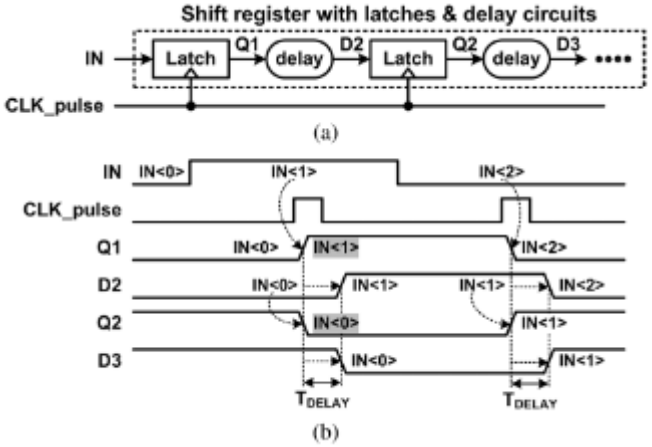

Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

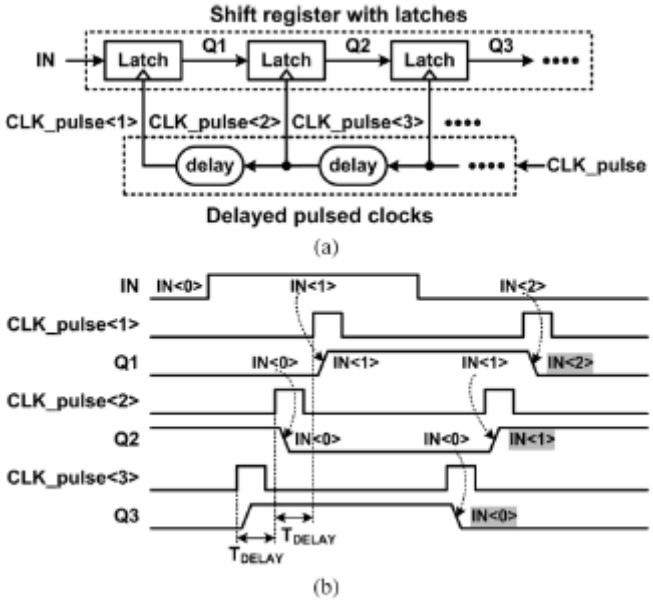

Fig.4. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

Fig. 5(a) shows an example the proposed shift register. The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals. In the 4-bit sub shift register #1, four

latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 5(b) shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal updates the latch data T1 from Q4. And then, the pulsed clock previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

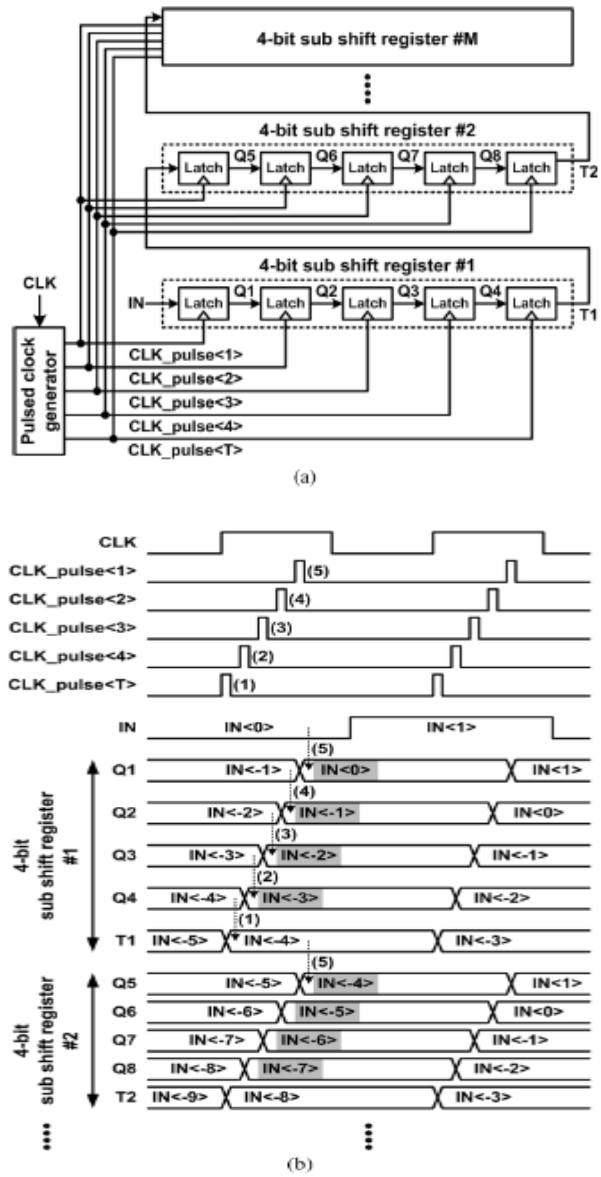

Fig.5. Proposed shift register. (a) Schematic. (b) Waveforms.

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig. 6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an N-bit shift register is divided into k-bit sub shift registers, the number of clock-pulse circuits is k+1and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1 latches requires K+1 pulsed clock signals. The number of sub shift registers becomes N/K, each sub shift register has a temporary storage latch. Therefore N/K latches are added for the temporary storage latches.

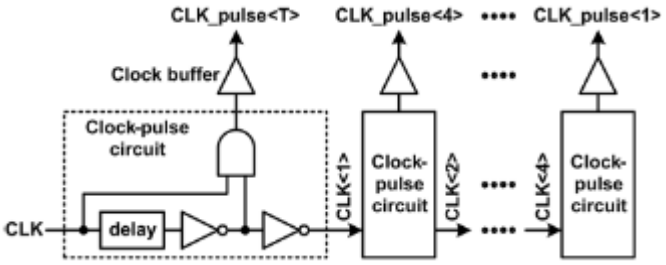

Fig.6. Delayed pulsed clock generator.

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip- flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 8, which is the smallest latch, is selected.

The original SSASPL with 9 transistors is modified to the SSASPL with 7 transistors in Fig.7 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.

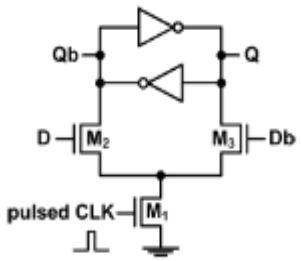

Fig.7. Schematic of the SSASPL.

Two 256-bit area-efficient shift registers using the SSASPL and PPCFF were implemented to show the effectiveness of the proposed shift register. Fig. 14 shows the schematic of the PPCFF, which is a typical master-slave flip-flop composed of two latches. The PPCFF consists of 16 transistors and has 8 transistors driven by clock signals. For a fair comparison, it uses the minimum size of transistors.

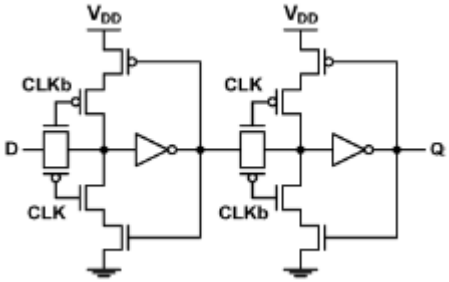

Fig.8. Schematic of the PPCFF.

III. EXPERIMENTAL RESULTS

Table I shows the transistor comparison of pulsed latches and flip-flops. When counting the total number of transistors in pulsed latches and flip-flops, the transistors for generating the differential clock signals and pulsed clock signals are not included because they are shared in all latches and flip-flops. The SSASPL uses 7 transistors, which is the smallest number of transistors among the pulsed latches.

The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops. The performance comparisons of the PPCFF and SSASPL is monitered. The SSASPL is 48.8% smaller and consumes 60.2% less power than the PPCFF.

Table 1

Transistor comparison of pulsed latches and flip-flops.

		Total number of transistors	Number of transistors connected to clock
Pulsed latch	**SSASPL [6]**	**7**	**1**
	TGPL [7]	10	4
	HLFF [8]	14	2
	CP3L [9]	26	6
Flip-flip	**PPCFF [10]**	**16**	**8**
	SAFF [11]	18	3
	DMFF [12]	22	5
	CPSA [13]	28	5
	CCFF [14]	28	5
	ACFF [15]	22	4

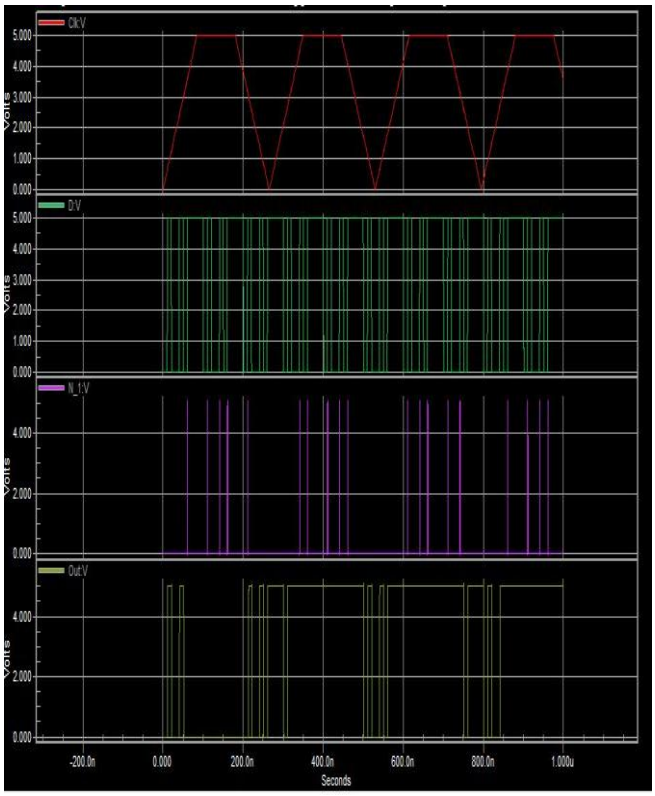

Fig.8. Schematic results of PPCFF.

IV. CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. The proposed shift register is designed by using tanner EDA and it saves 37% area and 44% power compared to the conventional shift register with flip-flops.

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